

# An Improved Active Front End Non-Regenerative Rectifier System Employing a Five-Limb Inductor

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**Abstract** — Variable frequency drives (VFDs) draw discontinuous current from the power system resulting in current distortion and consequently voltage distortion. Limiting current distortion to levels recommended in IEEE 519-1992 improves system efficiency, increases reliability, and limits voltage distortion that can adversely influence sensitive loads.

This paper revisits a non regenerative active front end system that has been studied in the past but offers significant improvements to make it acceptable to the drives industry. A three-phase current injecting inductor, required in the topology, is constructed in a five limb fashion and is shown to be helpful in limiting non characteristic harmonics. Since the current injected into the split dc bus capacitor is a 360Hz ripple, it is proposed that the main dc bus capacitor be split into film capacitor for ripple current and optimally reduced electrolytic capacitor for the main energy storage requirements. Experimental results are given based on the suggested improvement and low distortion levels that were not achieved in the past have been shown to be attainable. Comparison between a standard three-limb inductor and a five-limb inductor is made to highlight the performance improvements achievable. Adoption of the topology for common dc bus applications is also proposed.

**Index Terms**—Active Harmonic Filter, Five-limb Inductor, Harmonic Mitigation, Non-regenerative Active Filter.

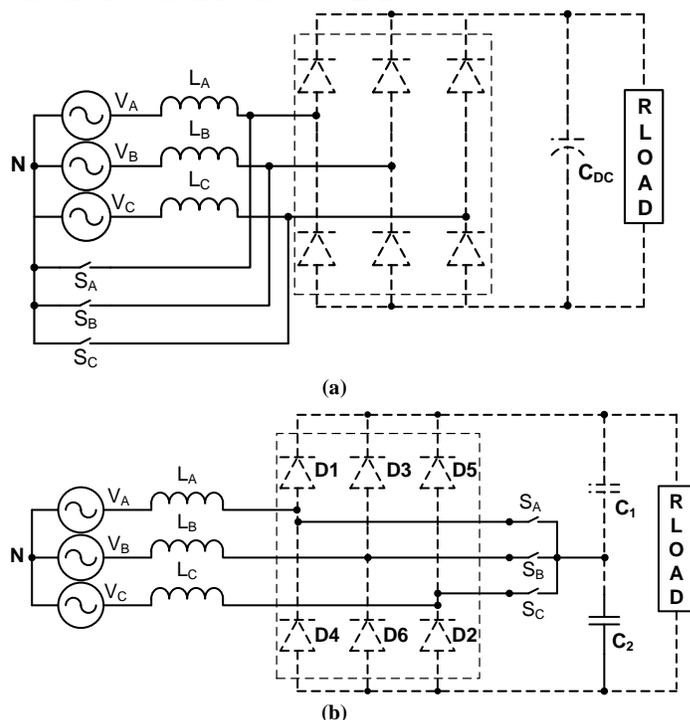
## I. INTRODUCTION

There are many techniques, both passive and active, that are employed to improve the input power factor of a VFD and reduce the overall current harmonics. The active techniques have an advantage over the passive techniques in size and performance. The cost of certain type of active techniques can be higher than passive technique.

This paper proposes improvements to a low cost active circuit that was reported in 1997 [2]. The basic circuit is shown in Fig. 1 and employs bidirectional switches that are rated to handle the harmonic compensation current only, which is about 35% of the rated current of the VFD. The circuit of Fig. 1 does not support regeneration. Since most HVAC applications do not need regeneration, bulky and expensive four quadrant converters are not needed.

The topology shown in Fig. 1 is a three-phase boost converter that forces current conduction in phases that do not carry current during a typical six-pulse operation. The boost

converter requires a boost inductor and since it is switched at twice the supply frequency, it is large in size, but there is no concern of additional conducted EMI.



**Fig. 1:** Non regenerative active front end circuit. (a) Original circuit; (b) Modified circuit [2].  $S_A$ ,  $S_B$ , and  $S_C$  are bidirectional switches.

Fig. 1(a) shows the original method that needed access to the neutral of input ac source. By splitting the dc bus to create a midpoint, the original circuit was modified [2] to the one shown in Fig. 1(b). This allows the implementation of the active filter circuit without the need to access the neutral of the ac source. The topology shown in Fig. 1(b) is very similar to the popular Vienna Rectifier [3]. Since the switches in Fig. 1 are rated to handle only the harmonic current, it is easy to scale this topology for large power applications. Bidirectional conduction can be obtained by using four diodes and an IGBT or two IGBTs configured in series with common emitter or common collector; or one could use two anti-parallel reverse blocking IGBTs. From a switch loss point of view, four diodes and a switch option is the worst while using reverse blocking IGBTs is the best.

## II. PRINCIPLE OF OPERATION

It is well known that there are six distinct diode pairs that conduct in one electrical cycle in a typical 3-phase ac to dc rectifier. Each conduction interval involves one pair of diodes and lasts 60 electrical degrees, which means that one phase does not conduct every 60 electrical degrees. Typical rectifier input waveforms are shown in Fig. 2.

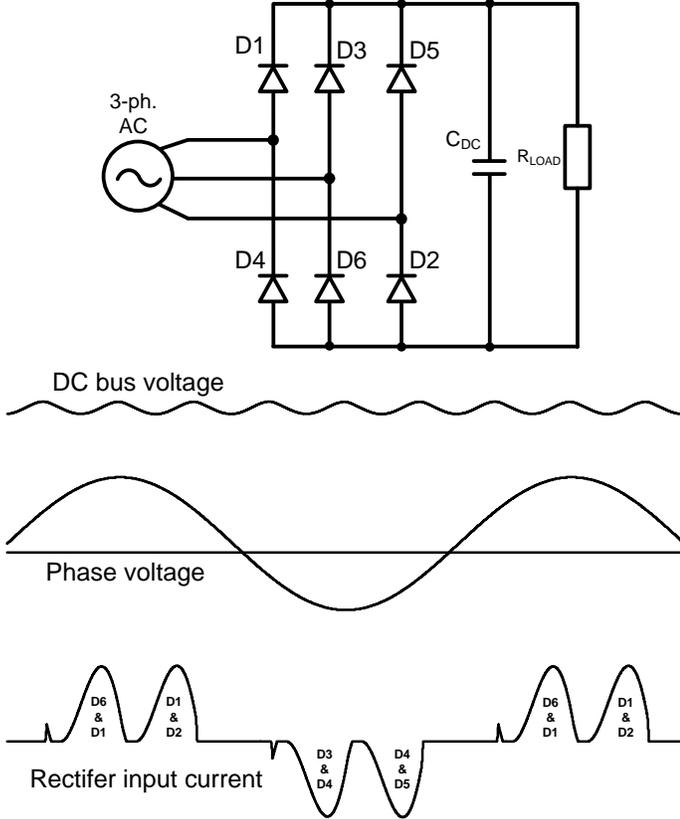


Fig. 2: A six pulse ac to dc rectifier system with its associated voltage and current waveforms.

By employing a switch, current can be forced through the non conducting phase into the midpoint of the dc bus. To store energy during this period, inductors are employed. The current through the non conducting phase is maintained until its turn to naturally conduct occurs. At that point, the switch is turned OFF. Turning OFF of the switch causes the energy in the inductor to be transferred to the dc bus similar to a boost converter. By turning ON and OFF the switch at the appropriate time (Fig. 3), continuous current can be maintained in all the phases.

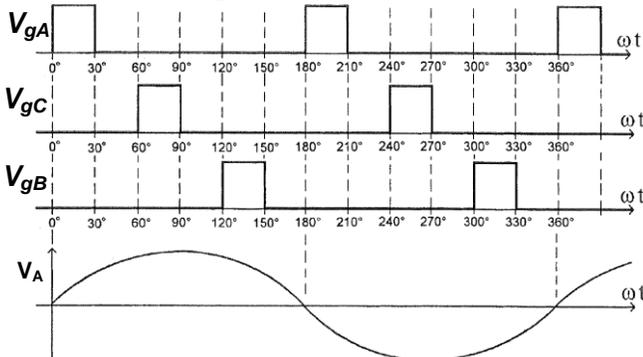


Fig. 3: Switching instances for the switches in Fig. 1(b) [2].

### A. Different Modes of Operation

In this subsection the operating modes of the circuit shown in Fig. 1(b) are discussed, concentrating on one half of the electrical cycle of phase A.

$0^\circ$  to  $30^\circ$

In Fig. 1(b),  $V_A$  is the line-neutral voltage corresponding to phase A. The switch connected to the inductor in phase A is turned ON at  $0^\circ$ . It remains ON for a maximum duration of  $30^\circ$  at which point, it is turned OFF. During the ON period, the inductor of phase A is connected to the mid-point of the dc bus formed by the split capacitors. This interval is shown in Fig. 4(a). Current increases in a co-sinusoidal manner through the inductor. During this interval, it is also assumed that diodes D5 and D6 are conducting. They remain in conduction during this interval.

$30^\circ$  to  $60^\circ$

At the end of the first interval, switch  $S_A$  is turned OFF and due to the inductance in the circuit, the current forward biases the diode connecting inductor  $L_A$  to the positive of the dc bus as shown in Fig. 4(b). During this interval, diode D1 starts conducting bringing the total number of diodes in conduction from two to three. Current continues to flow through phase A.  $60^\circ$  to  $90^\circ$

During this interval, diode D3 stops conducting since switch  $S_C$  in phase C is turned ON per the sequence shown in Fig. 3. Current in Phase C reverses since the midpoint voltage is higher than the instantaneous voltage of Phase C. Current continues to flow through Phase A and returns via Phase B. Fig. 4(c) is the equivalent circuit during this interval.  $90^\circ$  to  $120^\circ$

$90^\circ$  to  $120^\circ$

At the end of the previous interval, switch  $S_C$  is turned OFF. Since current through the inductor  $L_C$  cannot be stopped abruptly, diode D2 connecting the inductor  $L_C$  to the negative bus gets forward biased and allows current to remain flowing through Phase C. Currents in Phases A and B continue to flow. Three diodes conduct in this interval – Fig. 4(d).  $120^\circ$  to  $150^\circ$

$120^\circ$  to  $150^\circ$

From Fig. 3, it is seen that during this time interval, switch  $S_B$  connecting Phase B to the midpoint of the dc bus capacitor needs to be turned ON. This turns OFF diode D6. Current in Phase B changes its direction since the voltage of Phase B is higher than the midpoint of the dc bus capacitor. During this interval, there are two diodes and one switch conducting, as shown in Fig. 4(e). Current in Phase A continues to flow.  $150^\circ$  to  $180^\circ$

$150^\circ$  to  $180^\circ$

Switch  $S_B$  connecting Phase B to the midpoint of the dc bus capacitor turns OFF at the beginning of this interval. Due to inductance in the circuit, current in Phase B continues to flow as diode D3 gets forward biased and connects inductor  $L_B$  to the positive of the dc bus as shown in Fig. 4(f). Current in phase A is now waning and is ready to change direction in the next interval.

The voltage stress across the switch is discussed later. It is shown that the stress across the switch depends on how the dc bus midpoint is configured.

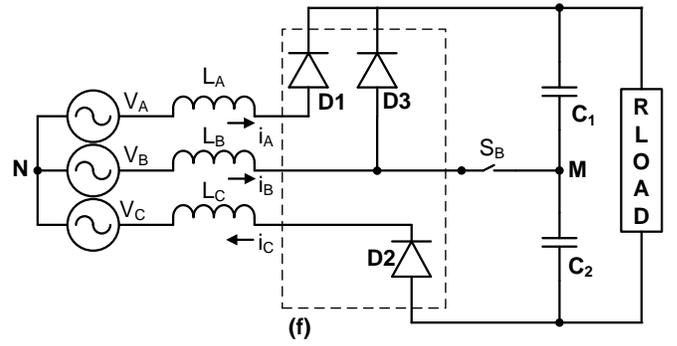
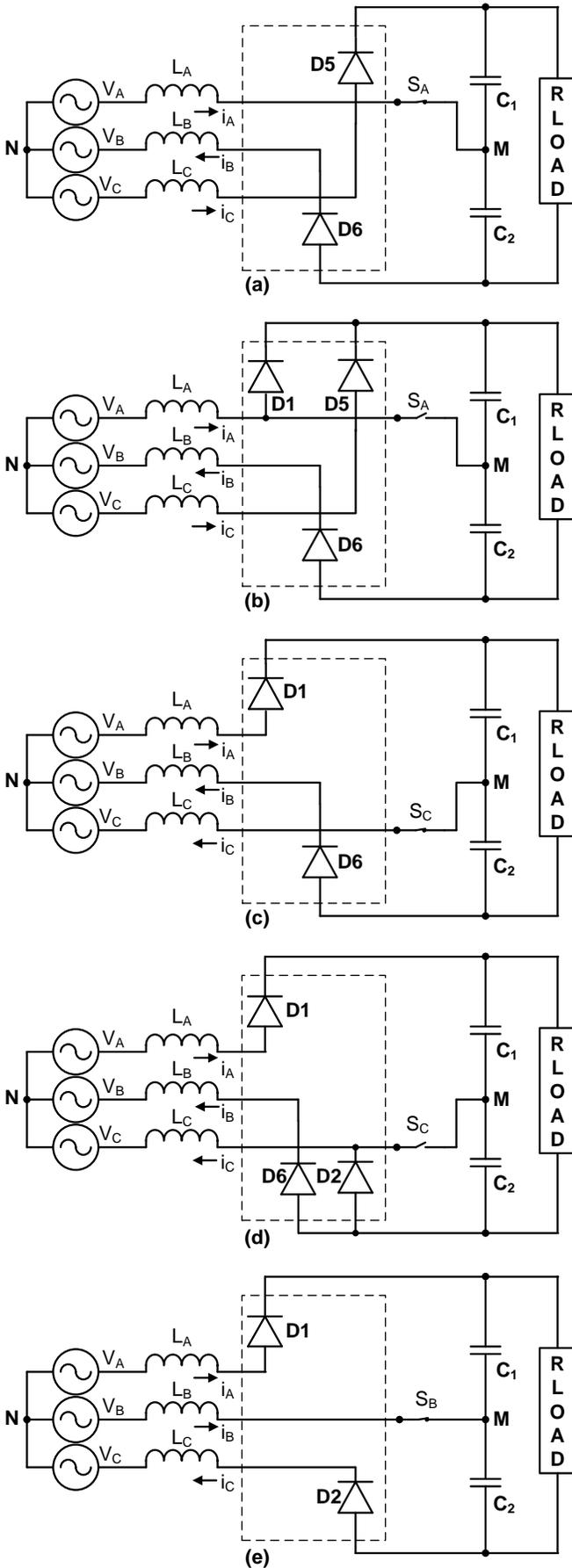


Fig. 4: Sequence of events during one half of the electrical cycle involving phase A.

### B. Inductor Design

The inductor is designed for rated current condition. By selecting the inductor appropriately, the current at the end of the switch conducting period is made equal to about one-half of the peak value of the rated current –  $I_m/2$ . This sets up the design equation for the inductor. During the  $0^\circ$  to  $30^\circ$  interval, it can be seen that voltage of point M in Fig 4(a) is same as the voltage of the neutral point N, since  $L_C$  is connected to the positive bus and  $L_B$  is connected to the negative bus. The equation for current flow through  $L_A$  during this interval is derived next. It will help in determining the value of inductor  $L_A$ . Inductors  $L_A$ ,  $L_B$ , and  $L_C$  are assumed to have the same inductance value  $L$ .  $V_m$  is the peak line-neutral voltage.

$$v_A = L \cdot \frac{di_A}{dt}$$

$$i = \int_0^t \frac{v_A}{L} \cdot dt = \int_0^{\theta} \frac{V_m \cdot \sin(\theta)}{\omega L} \cdot d\theta$$

$$i = \frac{V_m}{\omega L} \cdot (1 - \cos(\theta))$$

At  $\theta = 30$ , the value of inductor current is assumed to reach  $I_m/2$

$$\frac{I_m}{2} = \frac{V_m}{\omega L} \cdot \left(1 - \frac{\sqrt{3}}{2}\right)$$

$$\frac{P_o}{3 \cdot V_m} = \frac{V_m}{\omega L} \cdot \left(1 - \frac{\sqrt{3}}{2}\right)$$

$$\omega L = \frac{3 \cdot V_m^2}{P_o} \cdot \left(1 - \frac{\sqrt{3}}{2}\right)$$

$$\omega L = 2 \cdot Z_{pu} \cdot (0.133)$$

$$\omega L \approx 0.266 \cdot Z_{pu} \quad (1)$$

## III. PROPOSED IMPROVEMENTS

### A. Five Limb Inductor Option

From equation (1), it is seen that the input inductor is large and is predicted to occupy much space. Single phase inductors are preferred over three-phase inductor since the single-phase inductors offer common mode impedance and

any preexisting imbalance in the source voltage will not create undue non-characteristic current harmonics. However, single-phase inductors occupy more space and the cost of three single-phase inductors is typically higher than the cost of one three-phase inductor. Given this fact, it is difficult to justify use of three single-phase inductors. However, as a compromise, a five-limb inductor is proposed to be used here. A five-limb inductor offers common mode impedance and can help reduce the influence of pre-existing voltage imbalance on the current harmonics flowing through the system.

In a typical three-limb inductor, the third harmonic flux cancels out and no third harmonic flux circulates in the core. In other words, it can be said that a typical three-limb inductor offers high reluctance to third harmonic flux. The high reluctance to third harmonic flux pushes the flux pattern more towards the fundamental. The slight increase in fundamental flux creates a higher fifth and seventh harmonic current when such inductors are used in a typical 3-phase ac to dc rectifier circuits. In other words, using a standard three-limb inductor can cause higher fifth and seventh harmonic current to flow due to pre-existing third harmonic voltage in the ac system. The pre-existing third harmonic voltage is typically due to pre-existing phase voltage imbalance.

If the inductor has a five limb core, the third harmonic flux will exist in the core since it has a path to flow. The flow of third harmonic current will influence the fundamental voltage in a way to reduce its value. The slight reduction in the fundamental voltage will reduce the fifth and seventh harmonic currents in the system when this inductor is used in front of a three-phase ac to dc rectifier circuit. By designing the reluctance of the path for the third harmonic flux in an optimal manner, it is possible to significantly reduce the fifth and seventh harmonic fluxes in the core. Fig. 5 shows how the third harmonic flux does not exist in a three-limb inductor and how a path can be provided for this flux in a five limb inductor. Experimental results shown later prove the benefit of using a five limb inductor in this topology.

### B. Separation of Ripple Current Capacitor from Electrolytic Capacitor

From the discussions in Section II on the operating modes, it is well understood that during the operation of the switch, a ripple current flows into and out of the dc bus midpoint. The current flows six times back and forth into and out of the dc bus midpoint. The 180Hz ripple current will have peak amplitude of one-half of the rated maximum current, as shown in equation (1). The current shape is shown in Fig. 6 and the rms value of the capacitor ripple current is derived next. From Fig. 6, the capacitor current can be defined as follows:

$$\begin{aligned}
 i_C &= I_m \cdot \sin(\theta) & 0 \leq \theta \leq \pi/6 \\
 &= 0 & \pi/6 < \theta < \pi/3 \\
 &= I_m \cdot \sin\left(\frac{\pi}{3} - \theta\right) & \pi/3 \leq \theta \leq \pi/2 \\
 &= 0 & \pi/2 < \theta < 2\pi/3
 \end{aligned} \tag{2}$$

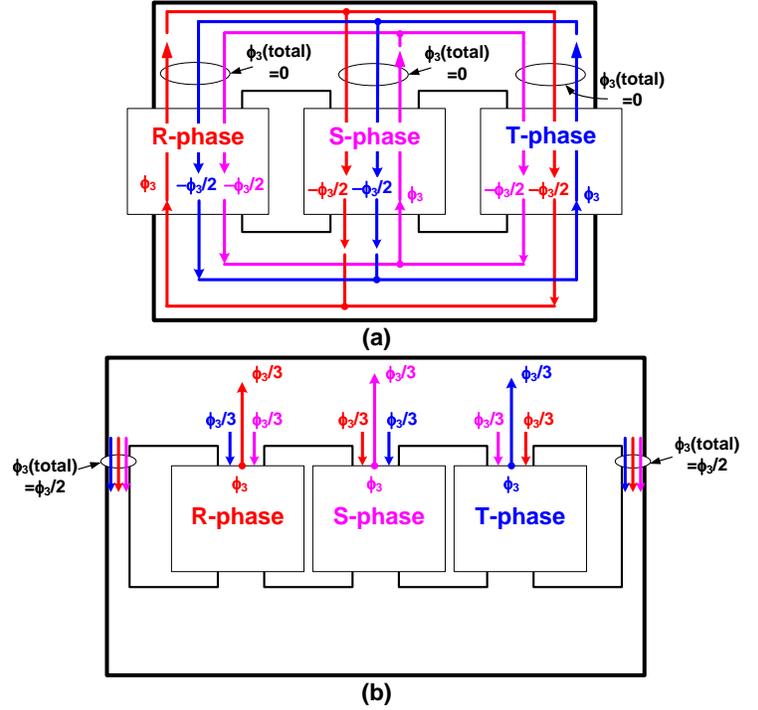


Fig. 5: a. Three-limb inductor with no third harmonic flux; b. Five limb inductor with third harmonic flux in the limbs and yokes.

Due to half-wave symmetry, the rms capacitor current can be computed as follows:

$$\begin{aligned}
 i_{Crms} &= \sqrt{\frac{3}{\pi} \cdot \int_0^{\pi/6} I_m^2 \cdot \sin^2(\theta) \cdot d\theta} \\
 i_{Crms} &= \sqrt{\frac{3 \cdot I_m^2}{2 \cdot \pi} \cdot \int_0^{\pi/6} (1 - \cos(2\theta)) \cdot d\theta} \\
 i_{Crms} &= \sqrt{\frac{3 \cdot I_m^2}{2 \cdot \pi} \cdot \left(\frac{\pi}{6} - \frac{\sin(\pi/3)}{2}\right)} \\
 i_{Crms} &\approx 0.208 \cdot I_m \approx 0.29 \cdot I_{in(rms)} \\
 i_{C1} = i_{C2} &= \frac{i_{Crms}}{\sqrt{2}} \approx 0.21 \cdot I_{in(rms)} \tag{3}
 \end{aligned}$$

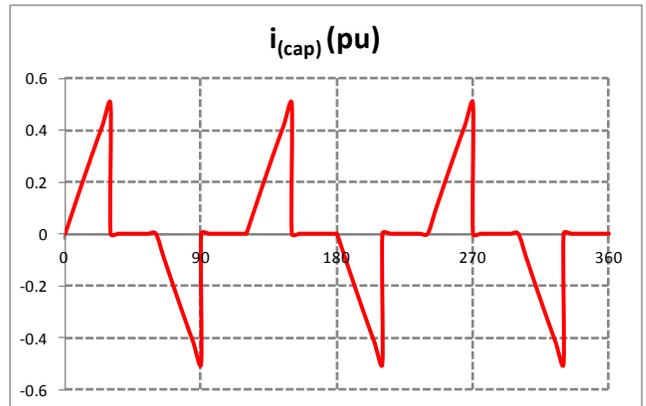


Fig. 6: Theoretical current flowing into the dc bus midpoint.

From (3), it is clear that the dc bus midpoint capacitors need to handle significant amount of ripple current. Typical electrolytic capacitors used in VFDs do not have high ripple current carrying capacity. In order to provide the necessary ripple current, many electrolytic capacitors need to be used in parallel. The use of multiple electrolytic capacitors across the dc bus increases the size and cost of VFDs. To alleviate this problem, it is proposed to separate the ripple handling capacitors from the bulk dc bus electrolytic capacitors. This would optimize the dc bus structure and reduce cost significantly. By separating the ripple handling capacitors from the bulk electrolytic capacitors, the voltage stress across the switches,  $S_A$ ,  $S_B$ , and  $S_C$  is greatly altered. The stress across the switches is discussed next.

If the dc bus midpoint was formed using big bulky electrolytic capacitors, the voltage across switch  $S_A$  would vary from close to zero when it is ON, to  $V_{DC}/2$  when it is OFF. However, due to the proposed separation of filter capacitor from the bulk electrolytic capacitors, the voltage across  $S_A$  is no longer stiff since the midpoint voltage moves depending on whether the midpoint is being charged or discharged.

During the first interval (Fig. 4(a)), switch  $S_A$  is ON and so the voltage across it is the on-state drop across the IGBT plus the conducting diode forward voltage drop. The total voltage is low across the conducting switch.

At the end of the first interval, switch  $S_A$  is turned OFF. Since the current through inductor  $L_A$  cannot stop flowing immediately, diode D1 gets forward biased and the inductor  $L_A$  gets pulled up to the positive dc bus. The collector of  $S_A$  comes close to  $V_{DC}$  but since the midpoint gets disconnected from all the phases, the midpoint voltage is held at the value it had at the end of the first interval. This voltage is close to  $V_m/2$  where  $V_m$  is the maximum value of the line-neutral voltage.  $V_m$  can be expressed in terms of  $V_{DC}$  as follows:

$$V_{DC} = \frac{3 \cdot \sqrt{3}}{\pi} \cdot V_m$$

$$V_m = 0.604 \cdot V_{DC} \quad (4)$$

Hence, voltage across  $S_A$  at the end of interval 1 is close to  $V_m/2$  or  $0.3V_{DC}$ .

At the end of the second interval, switch  $S_C$  turns ON and the midpoint discharges into phase C. The voltage across switch  $S_A$  increases since the collector of  $S_A$  is still connected to inductor  $L_A$ . The voltage across  $S_A$  increases in a quasi sinusoidal manner from  $V_m/2$  to  $3V_m/2$  or from  $0.3V_{DC}$  to  $0.9V_{DC}$  ( $v_A - v_C$  at  $\theta = 90^\circ$ ) as experimental results show.

During the  $90^\circ$  to  $120^\circ$  interval, the midpoint gets disconnected from the switches and is neither being charged nor discharged. The voltage across  $S_A$  remains at the value that is had at the end of the previous interval  $-0.9V_{DC}$ .

From  $120^\circ$  to  $150^\circ$ , the midpoint gets charged from phase B since switch  $S_B$  turns ON. The voltage across switch  $S_A$  starts

falling down since midpoint voltage moves up along with phase B voltage,  $v_B$ . The voltage across switch  $S_A$  moves down from an initial value of  $0.9V_{DC}$ , following a path carved by  $v_A - v_B$ . The final voltage across switch  $S_A$  is thus computed to be  $(3V_m/2 - \sqrt{3}V_m/2)$  or  $0.38V_{DC}$ .

Finally, from  $150^\circ$  to  $180^\circ$ , the midpoint remains disconnected from all the three phases and so the voltage across switch  $S_A$  remains at  $0.38V_{DC}$ . In the subsequent interval, the voltage across  $S_A$  is close to zero since switch  $S_A$  turns ON to discharge the midpoint voltage into phase A.

### C. Adapting to Delta Connected Source

All the explanations including the various intervals of operation have been explained assuming that the source is connected in a wye configuration with a floating neutral. In many industrial applications, the source can be connected in delta. This would require the logic controller to accommodate the desired phase shift. A low cost method to achieve the desired phase shift of 30 electrical degrees is proposed here. For a given operating condition if the conduction angle is  $\alpha$  with the input configured in wye, then it will need to be  $30 + \alpha$  when the input is configured in delta. To accommodate this, a high impedance resistor network configured in wye is used. The phase to neutral voltage out of the 3-phase resistor network is used as the reference voltage for zero crossing. This phase shifted voltage reference yields the desired 30 degrees phase shifted needed to accommodate ac sources configured in delta. If the input is already configured in wye, the output from the resistor network does not undergo any phase shift and so the resistor network can remain irrespective of the configuration of the input ac source. The vector representation of the delta system and the corresponding phase shift achieved using a wye configured resistor network is shown in Fig. 7.

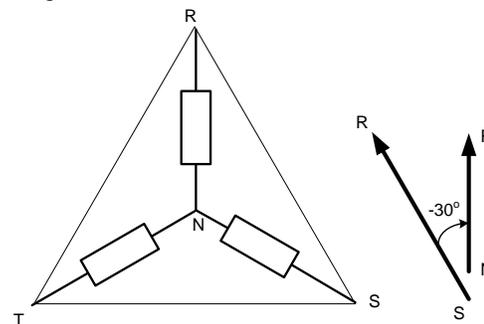


Fig. 7: Phase shifting scheme to achieve the desired 30 degree phase shift to accommodate delta connected source using a wye connected resistor network.

### D. Change in location of Current Sensor

The original topology discussed in [4] uses a current sensor in the dc bus to allow for power control. However, the emphasis in the modified topology is towards dc bus voltage control rather than dc bus power control. This change in strategy is geared towards the main objective of using the active front end topology for VFD loads fed from a regulated dc voltage. The VFD itself is typically equipped with sophisticated algorithms to control speed and torque in ac motors and so the active front end converter need not be

burdened with power control. It is thus proposed here to remove the current sensor from the dc bus and use a current sensor to sense the dc bus midpoint current to protect the switches due to abnormal operating condition. Hence, the ripple current into the midpoint of the dc bus capacitor is monitored and is used as a protection feature to reduce  $\alpha$  in cases where the current exceeds the designed maximum value. By changing the current monitoring location and its purpose from regulation to protection, the rating and cost of the current sensor is significantly reduced.

#### E. Use of Topology in Common dc Bus Applications

By separating the ripple carrying capacitor from the main electrolytic capacitors and by changing the role of the current sensor from power control to protection which facilitated its move from dc link to dc bus midpoint, it is possible to have an active front end topology that has three phase ac as input and a regulated dc bus voltage as the output. This proposal helps in optimizing the size and cost of the active front end system to make it power multiple VFDs on a common dc bus. Such a topological modification is shown in Fig. 8.

### IV. TEST RESULTS

All of the improvements suggested above have been adopted in the unit tested. The schematic of the test setup is shown in Fig. 9. The components used are listed below.

#### A. Components Used

1.  $L_{in} = 0.64\text{mH}$ , 171Arms, a. 3-limb inductor; b. 5-limb inductor
2.  $C1 \sim C4 = 220\mu\text{F}$ , 700Vdc (Filter Capacitors)
3. DCCT: HC-TN45V4B15 (45AT = 4V) – (lower current rating than old method)
4.  $U1 \sim U3$ : Active Switch modules – QIA1215001-ES (Custom Module from Powerex 150A, 1200V)
5. Snubber Capacitors (not shown in Fig. 9) rated at  $0.22\mu\text{F}$ , 600Vdc across  $U1$ ,  $U2$ , and  $U3$  are employed.

#### B. Test Plan and Test Results

A system rated at 240V, 75hp was built and was tested at various power conditions. The test setup is shown in Fig. 9. Following tests were conducted:

- A. 75hp rated system was tested at 38hp load corresponding to approximately 50% power;
- B. 75hp rated system was tested at 56hp load corresponding to approximately 75% power; and
- C. 75hp rated system was tested at 75hp load corresponding to 100% power;

At the test points, the input current and voltage THD were measured. The dc bus voltage regulation was also monitored. The dc bus was regulated to be at about 316Vdc. Test results are shown in Figs. 10 and 11. The results are tabulated in Tables 1 and 2, where TDD is defined as the ratio of harmonic current to the NEC rated current for the AC motor.

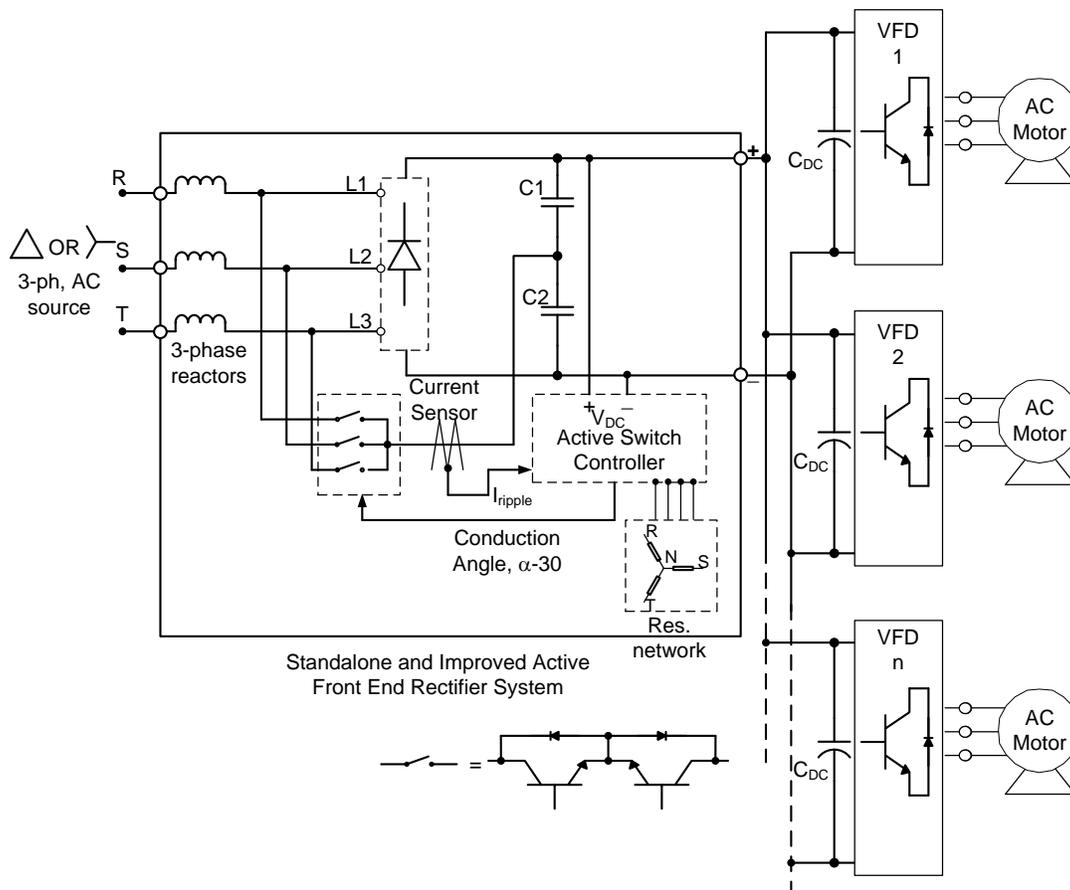
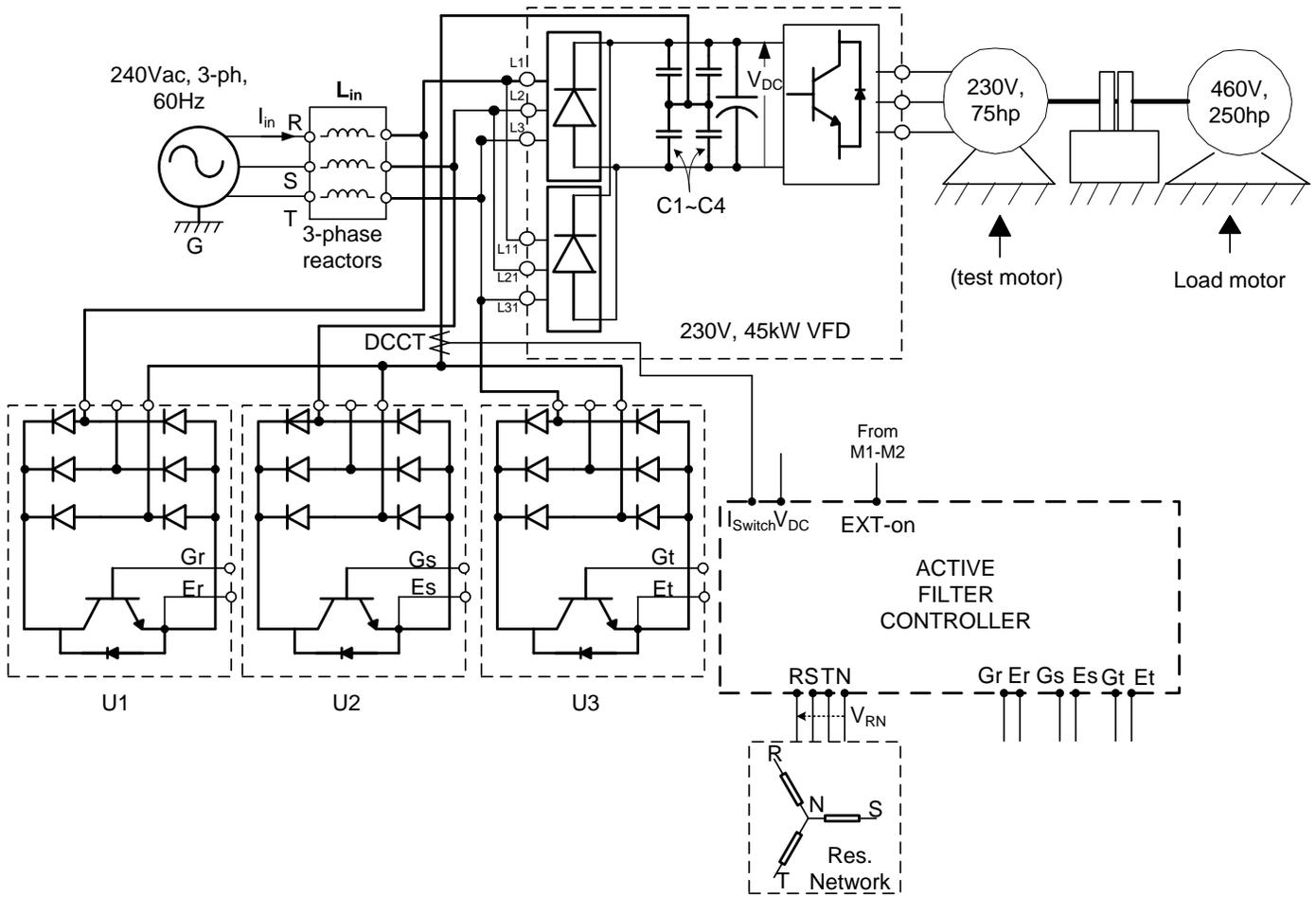


Fig. 8: Schematic of proposed circuit for common dc bus implementation.



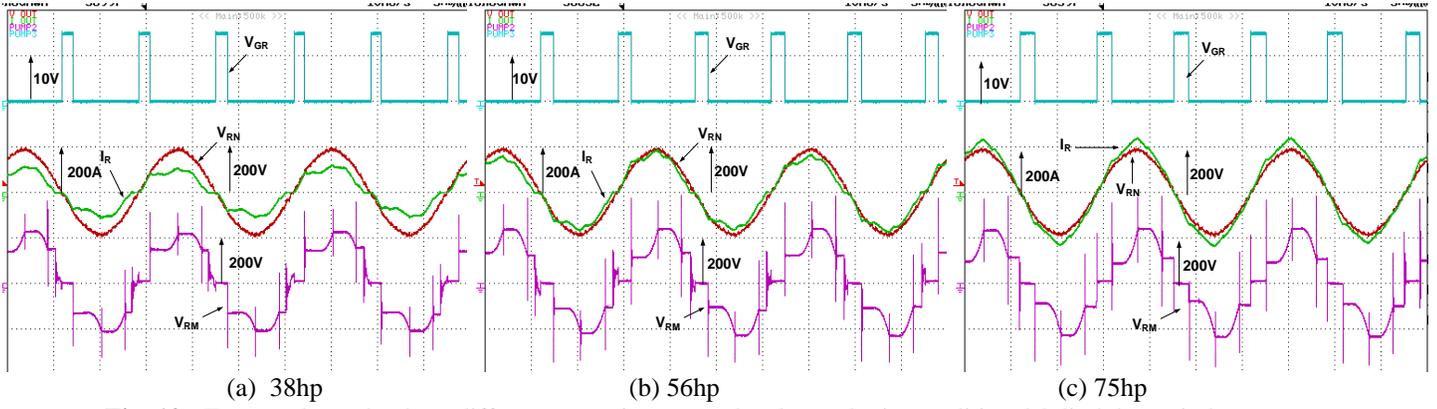
**Fig. 9:** Test circuit setup.

**Table 1:** Harmonic data for the 240V, 75hp, non regenerative active front end converter system

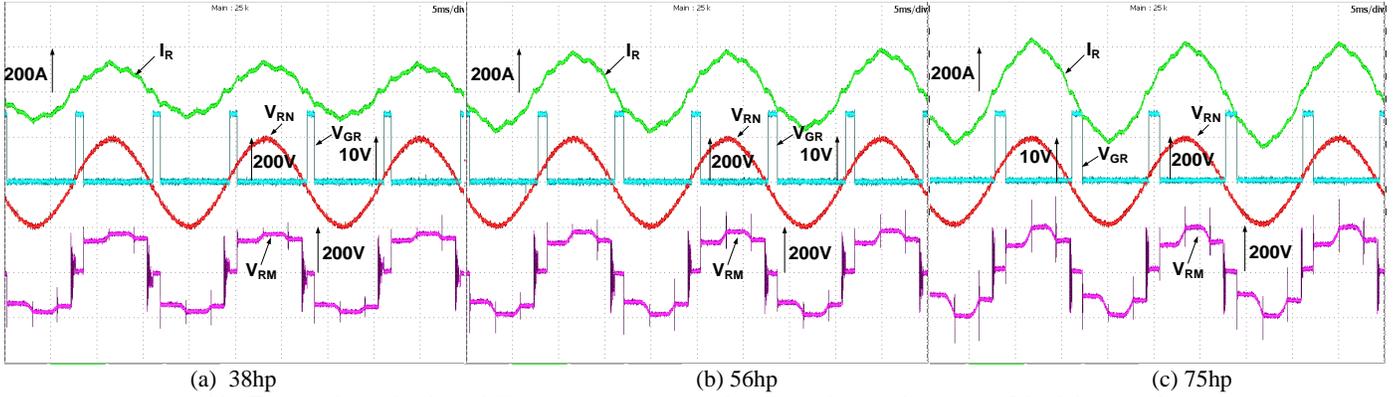
| Load (hp) | $I_R$ (A) |        | $I_3$ (A) |            | $I_5$ (A) |            | $I_7$ (A) |            | $I_9$ (A) |            | $I_{11}$ (A) |            | $I_{13}$ (A) |            | $I_{17}$ (A) |            |
|-----------|-----------|--------|-----------|------------|-----------|------------|-----------|------------|-----------|------------|--------------|------------|--------------|------------|--------------|------------|
|           | 3-limb    | 5-limb | 3-limb    | 5-limb     | 3-limb    | 5-limb     | 3-limb    | 5-limb     | 3-limb    | 5-limb     | 3-limb       | 5-limb     | 3-limb       | 5-limb     | 3-limb       | 5-limb     |
| 38        | 77.5      | 79.1   | 5.6       | <b>1.7</b> | 7.3       | <b>4.1</b> | 4.9       | <b>3.1</b> | 0.8       | 0.8        | 2.1          | <b>4.6</b> | 0.3          | <b>2.7</b> | 1.2          | <b>0.5</b> |
| 56        | 117.8     | 115.4  | 2.6       | <b>1.1</b> | 6.6       | <b>4.4</b> | 5.6       | <b>3.3</b> | 1.2       | <b>1.1</b> | 2.6          | <b>4.7</b> | 0.3          | <b>2.7</b> | 1.9          | <b>0.4</b> |
| 75        | 154.2     | 153.2  | 1.6       | <b>1.0</b> | 5.1       | <b>4.6</b> | 3.4       | <b>4.1</b> | 1.6       | <b>0.6</b> | 3.3          | <b>3.7</b> | 0.8          | <b>1.1</b> | 1.1          | <b>1.0</b> |

**Table 2:** Summary block of harmonic data for the 240V, 75hp, non regenerative active front end converter system – NEC Rated Amps= 192A (used for computing TDD)

| Load (hp) | $V_{RN}$ (V) |        | Voltage THD (%) |            | Current THD% (TDD%) |                  |
|-----------|--------------|--------|-----------------|------------|---------------------|------------------|
|           | 3-limb       | 5-limb | 3-limb          | 5-limb     | 3-limb              | 5-limb           |
| 38        | 130.7        | 136.1  | 1.5             | <b>1.3</b> | 14.2 (5.7)          | <b>9.9 (4.1)</b> |
| 56        | 130.3        | 135.8  | 1.4             | <b>1.3</b> | 8.4 (5.1)           | <b>7.0 (4.2)</b> |
| 75        | 129.4        | 134.0  | 1.7             | <b>1.2</b> | 4.9 (3.9)           | 4.9 (3.9)        |



**Fig. 10:** Test results at the three different operating power levels employing traditional 3-limb boost inductor



**Fig. 11:** Test results at the three different operating power levels employing the custom 5-limb boost inductor

### C. Power Loss Comparison

The effect of using a five-limb structure to circulate the third order harmonics through the core can be observed in the power loss measurements. Experimental loss measurements are given here that show that the power loss increases when the five limb structure is used mainly because of the higher core loss. Though core loss was not specifically measured, everything remaining the same, one can say that the higher observed loss is primarily due to harmonic flux in the core. Table 3 shows the loss results.

**Table 3:** System efficiency test results

| $P_{\text{shaft}}$ | Pin for 3-limb | Pin for 5-limb | System eff. for 3-limb | System eff. for 5-limb |
|--------------------|----------------|----------------|------------------------|------------------------|
| 38hp (28.35kW)     | 30.45kW        | 32.19kW        | 93.1%                  | 88.1%                  |
| 56hp (41.77kW)     | 46.76kW        | 47.15kW        | 89.3%                  | 88.6%                  |
| 75hp (55.95kW)     | 60.03kW        | 62.51kW        | 93.2%                  | 89.5%                  |

### V. CONCLUSIONS

From the discussions above, the following important conclusions are made:

- The five-limb inductor is seen to perform well and is shown to reduce third order harmonics;
- Separating the filter capacitor from the electrolytic capacitors reduced the main dc capacitors by 33% ;
- The inductance used is 0.64mH - 0.287pu.

- The new current sensor location does not interfere with the operation of the circuit. Sensor rating is lower and so is less expensive;
- The proposed wye connected resistive voltage sensor network is seen to create the proper phase shift;
- The input current at rated load condition is seen to be about 155A, which is much less than the NEMA rating. This is because of the improved power factor. Lower value of input rms current significantly reduces loss in the power system, which is a primary motivation for active filtering;
- Power measurement shows that the five-limb structure incurs more loss than the traditional 3-limb structure. This is primarily due to higher core loss in the five limb structure since the core in the five limb structure has to handle the third order harmonic flux.

### REFERENCES

- [1] "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems", IEEE Std. 519-1992.
- [2] Evaldo L. M. Mehl, and Ivo Barbi, "An Improved High-Power Factor and Low-Cost Three Phase Rectifier", *IEEE Trans. on Industry Applications*, Vo. 33, No. 2, March/April 1997, pp: 485-492.
- [3] J.W. Kolar, H. Ertl, F.C. Zach, "Design and Experimental Investigation of a Three-Phase High Power Density High Efficiency Unity Power Factor PWM (VIENNA)Rectifier Employing a Novel Integrated Power Semiconductor Module", 11th Annual APEC Conference Proceedings, Vol. 2, pp.514-523, 1996.
- [4] Ali I. Maswood, and Fangrui Liu, "A Novel Unity Power Factor Input Stage for AC Drive Applications", *IEEE Trans. on Power Electronics*, Vol. 20, No. 4, July 2005, pp: 839-846.
- [5] Mahesh Swamy, "Three Phase Active Rectifier System", USPTO Application: 13/347,097, 10 January 2012.